

**SYSTEM AND METHOD FOR MINIMIZING INCREASES
IN VIA RESISTANCE BY APPLYING A NITROGEN
PLASMA AFTER A TITANIUM LINER DEPOSITION**

TECHNICAL FIELD OF THE INVENTION

[0001] The present invention is generally directed to manufacturing technology for semiconductor devices and, in particular, to a system and method for minimizing increases in via resistance during the manufacture of a semiconductor device.

BACKGROUND OF THE INVENTION

[0002] It is common for the electrical resistance of a via in a semiconductor device to increase slightly after a process induced thermal cycle such as a film deposition. However, a via in certain types of prior art semiconductor devices can sometimes exhibit a significant increase in via resistance during a subsequent thermal cycle. In some cases the increase in the electrical resistance of a via can range from twenty percent (20%) up to as much as one hundred fifty percent (150%). In addition, a via in some types of prior art semiconductor devices can also sometimes significantly expand in volume after a process induced thermal cycle.

[0003] One cause of the observed increase in the electrical resistance of the via and the observed volume expansion of the via is the presence of a fluorine contaminant embedded in a layer of

anti-reflective coating (ARC) titanium nitride (TiN) in the semiconductor device. The fluorine contaminant becomes embedded in the ARC TiN layer during an etch process for a via passage that partially etches into the ARC TiN layer. The fluorine chemically reacts with a layer of titanium during subsequent thermal process steps to form a titanium fluoride compound.

[0004] The titanium fluoride compound exhibits an increased electrical resistance and an increase in volume. The presence of the titanium fluoride compound increases the electrical resistance of the via. In addition, the presence of the titanium fluoride compound contributes to an undesirable increase in via volume.

[0005] Therefore, there is a need in the art for a system and method for minimizing increases in via resistance during the manufacture of a semiconductor device. There is also a need in the art for a system and method for ensuring that a fluorine contaminant will not chemically react to form a titanium fluoride compound in a via of a semiconductor device.

SUMMARY OF THE INVENTION

[0006] To address the above-discussed deficiencies of the prior art, it is a primary object of the present invention to provide a system and method for minimizing increases in via resistance of a semiconductor device.

[0007] In one advantageous embodiment of the present invention a via in a semiconductor device is formed by placing a metal layer on a substrate and placing a layer of anti-reflective coating (ARC) titanium nitride (TiN) over the metal layer. A layer of dielectric material is then placed over the ARC TiN layer. A mask and etch procedure is then performed to etch through the layer of dielectric material and to etch partially through the ARC TiN layer. The etched portions of the dielectric material and the etch portions of the ARC TiN layer form a via passage.

[0008] A titanium layer is then deposited over the exposed portions of the layer of dielectric material and over the exposed portions of the ARC TiN layer. The titanium layer is then subjected to a nitrogen plasma process. The nitrogen plasma converts the titanium layer to a first layer of titanium nitride. The first layer of titanium nitride does not react with fluorine. Therefore any fluorine that may be present within the ARC TiN layer will not react with the first layer of titanium nitride. This means that the electrical resistance and volume of the first layer of titanium

nitride will not significantly increase during subsequent thermal cycles.

[0009] A second layer of titanium nitride is then deposited on the first layer of titanium nitride. Then a layer of tungsten is deposited on the second layer titanium nitride. The layer of tungsten fills the via passage to form an electrical connection between the metal layer that is located under the layer of dielectric material and the tungsten layer that is located over the layer of dielectric material.

[0010] It is an object of the present invention to provide a system and method for minimizing increases in via resistance of a semiconductor device.

[0011] It is also an object of the present invention to provide a system and method for minimizing increases in via resistance of a semiconductor device by applying a nitrogen plasma after a titanium liner deposition.

[0012] It is yet another object of the present invention to provide a system and method for minimizing increases in via resistance of a semiconductor device by applying a nitrogen plasma to a layer of titanium material to convert the layer of titanium material to a first layer of titanium nitride.

[0013] It is still another object of the present invention to provide a system and method for minimizing increases in via

resistance of a semiconductor device by applying a nitrogen plasma to a layer of titanium material to convert the layer of titanium material to a first layer of titanium nitride so that fluorine will not chemically react with the first layer of titanium nitride.

[0014] The foregoing has outlined rather broadly the features and technical advantages of the present invention so that those skilled in the art may better understand the detailed description of the invention that follows. Additional features and advantages of the invention will be described hereinafter that form the subject of the claims of the invention. Those skilled in the art should appreciate that they may readily use the conception and the specific embodiment disclosed as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the invention in its broadest form.

[0015] Before undertaking the Detailed Description of the Invention below, it may be advantageous to set forth definitions of certain words and phrases used throughout this patent document: the terms "include" and "comprise," as well as derivatives thereof, mean inclusion without limitation; the term "or," is inclusive, meaning and/or; the phrases "associated with" and "associated therewith," as well as derivatives thereof, may mean to include, be

included within, interconnect with, contain, be contained within, connect to or with, couple to or with, be communicable with, cooperate with, interleave, juxtapose, be proximate to, be bound to or with, have, have a property of, or the like; and the term "controller" means any device, system or part thereof that controls at least one operation, such a device may be implemented in hardware, firmware or software, or some combination of at least two of the same. It should be noted that the functionality associated with any particular controller may be centralized or distributed, whether locally or remotely. Definitions for certain words and phrases are provided throughout this patent document, those of ordinary skill in the art should understand that in many, if not most instances, such definitions apply to prior uses, as well as future uses, of such defined words and phrases.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] For a more complete understanding of the present invention and its advantages, reference is now made to the following description taken in conjunction with the accompanying drawings, in which like reference numerals represent like parts:

[0017] FIGURE 1 illustrates a prior art structure of a semiconductor device in which a via is to be formed comprising a substrate, a metal layer, an anti-reflective coating (ARC) titanium nitride (TiN) layer, and a dielectric layer;

[0018] FIGURE 2 illustrates the prior art structure shown in FIGURE 1 in which an opening for a via has been etched through the dielectric layer and partially etched through the ARC TiN layer;

[0019] FIGURE 3 illustrates the prior art structure shown in FIGURE 2 in which a layer of titanium has been applied to the exposed surfaces of the dielectric layer and to the exposed surface of the ARC TiN layer;

[0020] FIGURE 4 illustrates the prior art structure shown in FIGURE 3 in which a layer of titanium nitride (TiN) has been applied to the exposed surfaces of the layer of titanium;

[0021] FIGURE 5 illustrates the prior art structure shown in FIGURE 4 in which a layer of tungsten has been applied to fill the via and to cover the exposed surfaces of the titanium layer;

[0022] FIGURE 6 illustrates the prior art structure shown in FIGURE 5 in which a contaminant from the ARC TiN layer has reacted with the layer of tungsten and caused the titanium to turn into a compound that has a high resistance and an expanded volume;

[0023] FIGURE 7 illustrates an advantageous embodiment of the invention in which a nitrogen plasma is applied to the prior art structure shown in FIGURE 3;

[0024] FIGURE 8 illustrates an advantageous embodiment of a structure for forming a via in a semiconductor device in accordance with the principles of the invention in which the application of the nitrogen plasma has converted the layer of titanium (Ti) to titanium nitride (TiN);

[0025] FIGURE 9 illustrates the structure of the invention shown in FIGURE 8 in which a second layer of titanium nitride (TiN) has been applied to the exposed surfaces of the first layer of titanium nitride (TiN);

[0026] FIGURE 10 illustrates the structure of the invention shown in FIGURE 9 in which a layer of tungsten has been applied to fill the via and to cover the exposed surfaces of the second layer of titanium nitride (TiN); and

[0027] FIGURE 11 illustrates a flow chart showing the steps of an advantageous embodiment of the method of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0028] FIGURES 1 through 11, discussed below, and the various embodiments used to describe the principles of the present invention in this patent document are by way of illustration only and should not be construed in any way to limit the scope of the invention. Those skilled in the art will understand that the principles of the present invention may be implemented in any type of suitably arranged semiconductor device.

[0029] To simplify the drawings the reference numerals from previous drawings may sometimes not be repeated for structures that have already been identified.

[0030] FIGURE 1 illustrates a prior art structure 100 of a semiconductor device in which a via is to be formed. Prior art structure 100 comprises a substrate 110. A metal layer 120 is placed on the substrate 110. Metal layer 120 serves as an interconnect metal that will connect the via (not shown in FIGURE 1) to other portions of the semiconductor device. An anti-reflective coating (ARC) titanium nitride (TiN) layer 130 is then placed on metal layer 120. A dielectric layer 140 (e.g., silicon dioxide) is then placed on the ART Tin layer 130.

[0031] Then a mask and etch procedure is employed to etch a via passage 200 through the prior art structure shown in FIGURE 1. As shown in FIGURE 2, the via passage 200 extends through the

dielectric layer 140 and partially into ARC TiN layer 130. The horizontal surface of the ARC TiN layer 130 that forms the base of via passage 200 is designated with reference numeral 210. After the via passage 200 has been etched, the via passage 200 is subjected to a via cleaning process.

[0032] Then a layer of titanium is applied to the surfaces of via passage 200. FIGURE 3 illustrates the prior art structure shown in FIGURE 2 in which a layer of titanium 310 has been applied to the exposed surfaces of the dielectric layer 140 and to the exposed surface 210 of the ARC TiN layer 130. The layer of titanium 310 is deposited by an Ionized Metal Plasma (IMP) procedure in a prior art titanium liner deposition chamber (not shown). For clarity, the thickness of the layer of titanium 310 in FIGURE 3 is not necessarily drawn to scale.

[0033] Then a layer of titanium nitride (TiN) is applied to the surfaces of the layer of titanium 310. FIGURE 4 illustrates the prior art structure shown in FIGURE 3 in which the layer of titanium nitride (TiN) 410 has been applied to the exposed surfaces of the layer of titanium 310. The layer of titanium nitride 410 is deposited by a Chemical Vapor Deposition (CVD) procedure in a prior art titanium nitride (TiN) liner deposition chamber (not shown). In order for the CVD procedure to operate properly, the prior art structure shown in FIGURE 3 must be heated in the CVD TiN chamber

to a temperature of approximately four hundred degrees Centigrade (400 °C) in an atmosphere of neutral nitrogen or an atmosphere of a mixture of nitrogen and helium. The CVD procedure deposits the layer of titanium nitride 410 as shown in FIGURE 4. For clarity, the thickness of the layer of titanium nitride 410 in FIGURE 4 is not necessarily drawn to scale.

[0034] In the next step, a layer of tungsten is deposited to fill the via passage 200. FIGURE 5 illustrates the prior art structure shown in FIGURE 4 in which a layer of tungsten 510 has been applied to fill the via passage 200 and to cover the exposed surfaces of the layer of titanium nitride 410. For clarity, the thickness of the layer of tungsten 510 in FIGURE 5 is not necessarily drawn to scale. The layer of tungsten 510 that fills via passage 200 provides an electrical connection from the interconnect metal layer 120 that is located beneath the dielectric layer 140 (through ARC TiN layer 130, and through the layer of titanium 310, and through the layer of titanium nitride 410) to the portions of the layer of tungsten 510 are located above the dielectric layer 140.

[0035] The inventors of the present invention have discovered that prior art structures of the type illustrated in FIGURE 5 sometimes display significant increases in via resistance during subsequent thermal cycles (e.g., film depositions). In some cases

the increases in the electrical resistance of the via ranged from twenty percent (20%) up to as much as one hundred fifty percent (150%). In addition, the inventors of the present invention have discovered that prior art structures of the type illustrated in FIGURE 5 also sometimes display significant volume expansion after the formation of the tungsten plug 510 within the via passage 200.

[0036] The inventors of the present invention have also discovered that one cause of the observed increase in the via resistance and the observed volume expansion is the presence of a contaminant embedded in the ARC TiN layer 130. The inventors have identified the contaminant as fluorine. The fluorine becomes embedded in the ARC TiN layer 130 during the via etch process that partially etches into the ARC TiN layer 130. The fluorine reacts with the layer of titanium 310 during subsequent thermal process steps to form a compound (e.g., a titanium fluoride compound). The compound so formed has an increased electrical resistance and volume expansion.

[0037] FIGURE 6 illustrates the prior art structure shown in FIGURE 5 in which a fluorine contaminant in the ARC TiN layer 130 has reacted with the overlying layer of tungsten 310. The presence of fluorine has caused a portion of the layer of titanium 310 to turn into a titanium fluoride compound 610. The titanium fluoride

compound 610 exhibits a high electrical resistance and an expanded volume. The volume expansion may deform the surrounding structures.

[0038] It is very desirable to be able to avoid the problems that are inherent in the types of prior art structures described above. The inventors of the present invention have discovered a system and method for minimizing the increases in via resistance and volume expansion.

[0039] The construction of an advantageous embodiment of the present invention follows the steps of the prior art method up to the deposition of the layer of titanium 310. FIGURE 7 illustrates an advantageous embodiment of the invention 700 that comprises the underlying prior art structure of FIGURE 3. The method of the present invention differs from the prior art method in that a nitrogen plasma (N^+) treatment is applied to the layer of titanium 310. The application of the nitrogen plasma is indicated in FIGURE 7 by arrow 710. The application of the nitrogen plasma treatment heats the structure 700 to a temperature of approximately four hundred degrees Centigrade (400 °C). The plasma treatment performs the heating function of the prior art pre-heating step.

[0040] The nitrogen plasma acts on the layer of titanium 310 and converts the layer of titanium 310 into a layer of titanium nitride (TiN). The layer of titanium nitride (TiN) is shown in FIGURE 8 and designated with the reference numeral 810. The layer of

titanium nitride (TiN) 810 may be referred to as a first layer of titanium nitride (TiN). For clarity, the thickness of the first layer of titanium nitride 810 in FIGURE 8 is not necessarily drawn to scale. At this point an optional gas stabilization step may be performed before undertaking the next step of the method.

[0041] Then a second layer of titanium nitride (TiN) is applied to the surfaces of the first layer of titanium nitride (TiN) 810. FIGURE 9 illustrates the structure 800 shown in FIGURE 8 in which a second layer of titanium nitride (TiN) 910 has been applied to the exposed surfaces of the first layer of titanium nitride (TiN) 810. The second layer of titanium nitride 910 is deposited by a Chemical Vapor Deposition (CVD) procedure in a prior art titanium nitride (TiN) liner deposition chamber (not shown). The CVD procedure deposits the second layer of titanium nitride 910 as shown in FIGURE 9. For clarity, the thickness of the second layer of titanium nitride 910 in FIGURE 9 is not necessarily drawn to scale.

[0042] In the next step, a layer of tungsten is deposited to fill the via passage. FIGURE 10 illustrates the structure 900 shown in FIGURE 9 in which a layer of tungsten 1010 has been applied to fill the via passage and to cover the exposed surfaces of the second layer of titanium nitride 910. For clarity, the thickness of the layer of tungsten 1010 in FIGURE 10 is not necessarily drawn to

scale. The layer of tungsten 1010 that fills via passage provides an electrical connection from the interconnect metal layer 120 that is located beneath the dielectric layer 140 (through ARC TiN layer 130, and through the first layer of titanium nitride 810, and through the second layer of titanium nitride 910) to the portions of the layer of tungsten 1010 are located above the dielectric layer 140.

[0043] The structure 1000 of the present invention illustrated in FIGURE 10 does not display significant increases in via resistance during subsequent thermal cycles and does not display volume expansion. This is because the first layer of titanium nitride (TiN) 810 does not react with fluorine. Therefore any fluorine contaminant in the ARC TiN layer 130 will remain embedded in the ARC TiN layer 130. Unlike the prior art case, there will be no formation of a titanium fluoride compound. This means that there will be no significant increase in via resistance and no volume expansion during subsequent thermal cycles.

[0044] FIGURE 11 illustrates a flow chart 1100 showing the steps of an advantageous embodiment of the method of the present invention. The method of the present invention begins by providing a substrate 110 of a semiconductor device 100 and placing a metal layer 120 over the substrate 110 (step 1110). In the next step an anti-reflective coating (ARC) titanium nitride (TiN) layer

130 (ARC TiN layer 130) is deposited over the metal layer 120 and the ARC TiN layer 130 is covered with a dielectric layer 140 (step 1120). Then a mask and etch procedure is performed to etch through the dielectric layer 140 and to partially etch through the ARC TiN layer 130 (step 1130). Then a layer of titanium 310 is deposited over exposed portions of dielectric layer 140 and over exposed portions of the ARC TiN layer 310 (step 1140).

[0045] Then a nitrogen plasma (N^+) process is applied to convert the layer of titanium 310 to a first layer of titanium nitride 810 (step 1150). Then a second layer of titanium nitride 910 is deposited over the first layer of titanium nitride 810 (step 1160). Then a layer of tungsten 1010 is deposited over the second layer of titanium nitride 910 and the via passage is filled with tungsten 1170 (step 1160). The method of the invention provides a via that exhibits no significant increase in electrical resistance and no significant volume expansion during subsequent thermal cycles.

[0046] Although the present invention has been described with an exemplary embodiment, various changes and modifications may be suggested to one skilled in the art. It is intended that the present invention encompass such changes and modifications as fall within the scope of the appended claims.